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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Larry Eugene Mosley
Title: MULTI-LAYER CHIP CAPACITOR
Attorney Docket No.: 884.240US1

PATENT APPLICATION TRANSMITTAL

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X Utility Patent Application under 37 CFR § 1.53(b) comprising:
- X Specification (13 pgs, including claims numbered 1 through 21 and a 1 page Abstract).
- X Formal Drawing(s) (5 sheets).
- X Signed Combined Declaration and Power of Attorney (3 pgs).
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X Assignment of the invention to Intel Corporation (2 pgs) and Recordation Form Cover Sheet.
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X Information Disclosure Statement (1 pgs), Form 1449 (1 pgs), and copies of cited references (3).
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INDEPENDENT CLAIMS	5 - 3 =	2	x 78 =	**$156.00**
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TOTAL				**$864.00**

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UNITED STATES PATENT APPLICATION

MULTI-LAYER CHIP CAPACITOR

INVENTOR

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Client Reference P8037

Multi-Layer Chip Capacitor

Technical Field of the Invention

The present invention relates generally to capacitors and in particular the present invention relates to multi-layer integrated circuit capacitors.

Background of the Invention

Integrated circuit devices operate using one or more power supplies. These power supplies traditionally have sufficient voltage and power to supply numerous circuits without interruption. Power supplies, however, have been decreasing in size. This forces the integrated circuit manufactures to decrease operating voltages and power requirements.

Under normal circumstances a power supply will be able to provide sufficient power to all circuits coupled to the supply. However, voltage drops on power supply lines can occur when there is a sudden increase in demand for power. This lower voltage can reduce switching times of the transistors in a circuit coupled to the supply. This in turn can cause a loss in performance of the circuit.

Decoupling capacitors can be provided in a circuit that is coupled to the power supply to minimize this voltage drop. That is, a decoupling capacitor stores a charge that helps stabilize changes in the voltage supply line. The response of these decoupling capacitors depends on the inductance and resistance of the capacitor and the amount of capacitance available. Fabricating decoupling capacitors in the same integrated circuit provides difficulty in obtaining sufficient capacitance for reliable decoupling.

An alternate approach is to provide numerous discrete capacitors external to a circuit package. These discrete capacitors are typically attached in parallel to a package, or circuit board. Physical space must be left between the capacitors for placement handling and soldering to the package. The spacing requires longer interconnect lines that results in higher inductance/resistance and less capacitance due to the wasted space

and the terminal spacing on the capacitors. In addition the capacitors have edge terminations that have higher inductance and resistance.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a decoupling capacitor that has more capacitance while controlling resistance and inductance characteristics.

Brief Description of the Drawings

Figure 1 illustrates a system of the present invention including a decoupling capacitor;

Figure 2 illustrates a cross-section view of one embodiment of a capacitor according to the present invention;

Figure 3 illustrates a top view of one embodiment of a capacitor according to the present invention;

Figure 4 illustrates a top view of one embodiment of a capacitor according to the present invention;

Figure 5 illustrates a cross-section view of another embodiment of a capacitor according to the present invention;

Figure 6 illustrates a cross-section view of another embodiment of a capacitor according to the present invention;

Figure 7 illustrates an embedded capacitor embodiment according to one embodiment of the present invention;

Figure 8 illustrates a cross-section view of another embodiment of a capacitor according to the present invention; and

Figure 9 illustrates an embedded capacitor package.

Detailed Description of the Invention

In the following detailed description of embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of

illustration specific embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the claims.

The present invention provides a multi layer thin film capacitor that can be used as a decoupling capacitor to stabilize a voltage provided by a power supply. The capacitor can be fabricated with inductance and resistance values typically seen only in thin film capacitors, but with the capability of obtaining a much higher capacitance. In one embodiment, the present invention provides a single discrete component that has a lower inductance and resistance due to increased contact locations on the capacitor body.

Many integrated circuits use a mounting technique based on controlled collapse chip connection (C4) sites. In the present invention, a large number of C4 sites decreases the resistance and the inductance of the capacitor because the current does not have to travel very far to reach a terminal. The C4 sites improve the performance of the capacitor as a decoupling capacitor. Techniques for mounting integrated circuits to circuit boards using C4 interconnects are well known in the art and a detailed description is not provided herein. The present invention allows a stand alone integrated circuit to be fabricated. Thus, real estate of an existing integrated circuit does not have to be sacrificed to include a relatively large decoupling capacitor.

Referring to Figure 1, a system 100 is generally illustrated that includes an integrated circuit 104, a power supply 102 and an external decoupling capacitor 106. The capacitor 106 is located external of the circuit 104 and fabricated as an integrated circuit device. In one embodiment, the capacitor is mounted on a circuit board 110, also called a package, physically adjacent to the circuit. The circuit board can be a mother board and circuit 104 can be a processor circuit. Both the circuit and the capacitor can be mounted to the package using C4 sites. In operation, the decoupling capacitor stores

a charge on its plates. This charge is then used to provide power if the supply (Vcc) drops. It is understood that the capacitor will discharge if the supply voltage drops too far or for an extended period of time. The decoupling capacitor, therefore, is intended to assist in maintaining an adequate voltage supply for short periods where the voltage supply may dip.

Figure 2 illustrates a cross-section of a capacitor of one embodiment of the present invention. The capacitor is fabricated on a substrate 202. Numerous layers of conductor 204 material separated by dielectric 208 are fabricated over the substrate. The conductive layers can be fabricated from any conductive material, such as but not limited to aluminum, copper or a metal alloy. The dielectric layers can be fabricated from any suitable dielectric, such as but not limited to $BaSrTiO_3$ (referred to herein as BST).

The BST and metal layers can be fabricated in layered strips, and alternating conductive layers are connected together. In an alternate embodiment, the BST and metal layers can be fabricated as full layers. Electrical connections are illustrated in Figure 2. It will be appreciated that the plates of the capacitor are interchangeable between Vcc and Vss connections of the power supply. The conductor and dielectric layers are covered with a dielectric material 206. This dielectric material can comprise, but is not limited to, the same material as dielectric layers 208. Vias 210 are fabricated through the dielectric material 206 to provide access to the conductive layers. The vias are then filled, or plated, with a conductive material to provide electrical interconnects to the conductive layers.

The number and size of the vias can be selected to reduce resistance of the capacitor interconnects and allow for C4 mounting to a package. The vias can be connected together in one of three ways. The first interconnect method includes fabricating conducting interconnects on a top surface of the capacitor. These interconnects can be conductive strips that run perpendicular to the conductive strip layers. A second embodiment provides interconnects on a package, or circuit board. The vias, therefore, are each coupled to the package. In a third embodiment, some of the vias are coupled using interconnect lines on the capacitor and some of the vias are

coupled using interconnect lines on the circuit board. Independent of how the vias are connected, lands (pads) can be made on the top of the capacitor to form C4 connections to attach to the package substrate.

Referring to Figure 3, a top-view, or plan view, of one embodiment of a capacitor is illustrated. The capacitor includes a plurality of C4 lands 220 located generally above the vias. The lands are staggered such that interconnect lines 240 and 242 connect to alternate conductive layers. The interconnect lines 240 and 242, in this embodiment are located on a circuit board that the capacitor mounts on.

An alternate embodiment is illustrated in Figure 4. In this embodiment, alternating interconnect lines 250 and 252 are fabricated on the top of the capacitor structure. The interconnect lines can include C4 lands to mount the capacitor to a circuit board. It will be appreciated by those in the art with the benefit of the present description that different interconnect patterns can be used with the present invention.

Referring to Figure 5, a cross-section of an alternate embodiment capacitor 300 is illustrated. While the embodiment of Figure 2 included strips of conductors that formed a pyramid-shaped cross-section, the present embodiment can be fabricated with full layers of conductors. The capacitor includes a substrate 302. A first layer of conductor 304 is located over the substrate. An second conductive layer 308 is separated from the first conductor by dielectric layer 306. Likewise dielectric layers 310 and 314 surround a top conductor 312. First electrical vias 316 are used to connect the first and third conductors. A clearance is provided in layer 308 to isolate the first vias from the second conductor layer. Second vias 318 contact the second conductive layer. Clearance areas are provided in the first conductor to isolate the second vias from the first conductor layer. C4 lands 320 can be provided to allow the capacitor to be mounted to a circuit board. In this embodiment the conductor layers do not decrease in surface area as the number of layers increase.

It will be recognized by those skilled in the art that the present invention can include a variety of capacitor plates having different patterns. That is, the capacitor plates can be fabricated in different patterns to accommodate different C4 arrangements, and the present invention should not be limited to the layouts described herein.

In another embodiment illustrated in Figure 6, the conductor layers are fabricated as described with reference to Figure 2. In this embodiment, however, the interconnect vias pass through the second conductor layer to connect both the top and bottom conductive layers using common vias. Again, a clearance area needs to be provided in the intermediate conductor to avoid shorts between the alternate conductor layers.

The present invention can be fabricated using known integrated circuit techniques. For example, the capacitor plates may be formed by any method, such as sputtering, chemical vapor deposition (CVD) or other deposition techniques. The top dielectric layer can be chemically/mechanically polished (CMP) to provide a planar surface for forming the C4 lands.

Figure 7 illustrates a cross section of an embedded capacitor embodiment comprising a capacitor 400 that is physically coupled to a dielectric layer 402. In one embodiment, the capacitor is attached to the dielectric using an adhesive. Vias 404 are then formed through the dielectric layer to expose electrical connections on the capacitor. The vias are then plated with a conductor to for an electrical interconnect to the capacitor. This embodiment, therefore, provides an alternate manner of coupling the capacitor to a circuit. Figure 8 illustrates another embodiment of the present invention where electrical vias 410 are formed through the substrate of the capacitor 400. The capacitor can be fabricated as explained herein, but with the additional electrical vias. These vias allow circuits to be coupled to both sides of the capacitor and provided a more direct conductive path between the circuits.

Figure 9 illustrates an embedded capacitor package 500. The capacitor 480 includes interconnect lands on each side of the capacitor and can be fabricated as illustrated in Figure 8. The capacitor has a first circuit package 450 formed on the top of the capacitor and a second package circuit 460 formed on the bottom of the capacitor. The packages have at least one conductive layer 440 and dielectric layers. The conductive layers are coupled using vias 440. These vias can be formed using a laser and plating the opening created with the laser. Other techniques can be used to fabricate

and connect the package layers. The embodiment of Figure 9, therefore, illustrates that the capacitor can be embedded in a multi-layer circuit package.

Conclusion

A thin film capacitor has been described that includes multiple layers of conductors separated by dielectric material. The conductive layers are connected to interconnect lands using conductive vias. The interconnect lands can be C4 lands that allow the capacitor to be connected to a circuit board. In one embodiment, the capacitor is mounted on a circuit board in close proximity to a processor circuit. The multi layer capacitor of the present invention provides the ability to increase a capacitance value while lowering interconnect resistance and inductance.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductor layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnect to the first, second and third conductor layers.

2. The multi layer integrated circuit capacitor of claim 1 further comprising a plurality of controlled collapse chip connection (C4) lands fabricated on the third insulator layer and in electrical contact with the plurality of conductive vias.

3. The multi layer integrated circuit capacitor of claim 2 wherein the C4 lands are fabricated in staggered columns in a plan view.

4. The multi layer integrated circuit capacitor of claim 1 wherein the conductor layers comprise a metal material and the insulator layers comprise $BaSrTiO_3$.

5. The multi layer integrated circuit capacitor of claim 4 wherein the conductor layers are fabricated from a copper.

6. The multi layer integrated circuit capacitor of claim 1 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer is patterned to form interconnect lines that selectively connect the plurality of plurality of conductive vias.

7. The multi layer integrated circuit capacitor of claim 1 wherein the second and third conductive layers are fabricated in a plurality of strips, such that a surface area of the second conductive layer is less than a surface area of the first conductive layer and a surface area of the third conductive layer is less than the surface area of the second conductive layer.

8. The multi layer integrated circuit capacitor of claim 1 wherein some of the plurality of conductive vias pass through the second conductive layer without forming an electrical connection with the second conductive layer.

9. A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer, the second conductive layer is fabricated as a plurality of laterally spaced strips such that a surface area of the second conductive layer is less than a surface area of the first conductive layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer, the third conductive layer is fabricated as a plurality of laterally spaced strips such that a surface area of the third conductive layer is less than the surface area of the second conductive layer;

a third insulator layer located over the third conductive layer;

a first plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnect to the third conductive layer;

a second plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnect to the second conductive layer; and

a third plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnect to the first conductive layer.

10. The multi layer integrated circuit capacitor of claim 9 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer is patterned to form interconnect lines that selectively connect the plurality of plurality of conductive vias.

11. A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer;

a first plurality of conductive vias downwardly extending through the third insulator layer, third conductive layer, second insulator layer, second conductive layer and the first insulator layer to provide electrical interconnect to the first and third conductive layers; and

a second plurality of conductive vias downwardly extending through the third insulator layer, third conductive layer and second insulator layer to provide electrical interconnect to the second conductive layer.

12. The multi layer integrated circuit capacitor of claim 11 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer is patterned to form interconnect lines that selectively connect the plurality of plurality of conductive vias.

13. The multi layer integrated circuit capacitor of claim 11 wherein the conductive layers comprise a metal material and the insulator layers comprise $BaSrTiO_3$.

14. A circuit package comprising:

a package having a pair of supply voltage interconnect lines;

a first integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines; and

a second integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines, the second integrated circuit package comprises a capacitor having:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnect to the first, second and third conductive layers.

15. The circuit board assembly of claim 14 wherein the second integrated circuit package comprises a plurality of controlled collapse chip connection (C4) lands that are electrically connected to the plurality of conductive vias and the supply voltage interconnect lines.

16. The circuit board assembly of claim 14 wherein the first integrated circuit package is a processor circuit.

17. The circuit board assembly of claim 14 wherein the conductive layers comprise a metal material and the insulator layers comprise $BaSrTiO_3$.

18. The circuit board assembly of claim 14 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer is patterned to form interconnect lines that selectively connect the plurality of plurality of conductive vias.

19. A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnect to the first, second and third conductive layers, the plurality of conductive vias further extend through the substrate to provide electrical interconnects on both a top and a bottom surface of the integrated circuit capacitor.

20. The multi layer integrated circuit capacitor of claim 19 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer is patterned to form interconnect lines that selectively connect the plurality of plurality of conductive vias.

21. The multi layer integrated circuit capacitor of claim 1 wherein the conductor layers comprise a metal material and the insulator layers comprise $BaSrTiO_3$.

Abstract of the Disclosure

An integrated circuit thin film capacitor includes multiple layers of conductors separated by dielectric material. The conductive layers are connected to interconnect lands using conductive vias. The interconnect lands can be controlled collapse chip connection (C4) lands that allow the capacitor to be connected to a circuit board. In one embodiment, the capacitor is mounted on a circuit board in close proximity to a processor circuit. The multi layer capacitor of the present invention provides the ability to increase a capacitance value while lowering interconnect resistance and inductance.

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Printed Name: Shawn Hise
Signature:

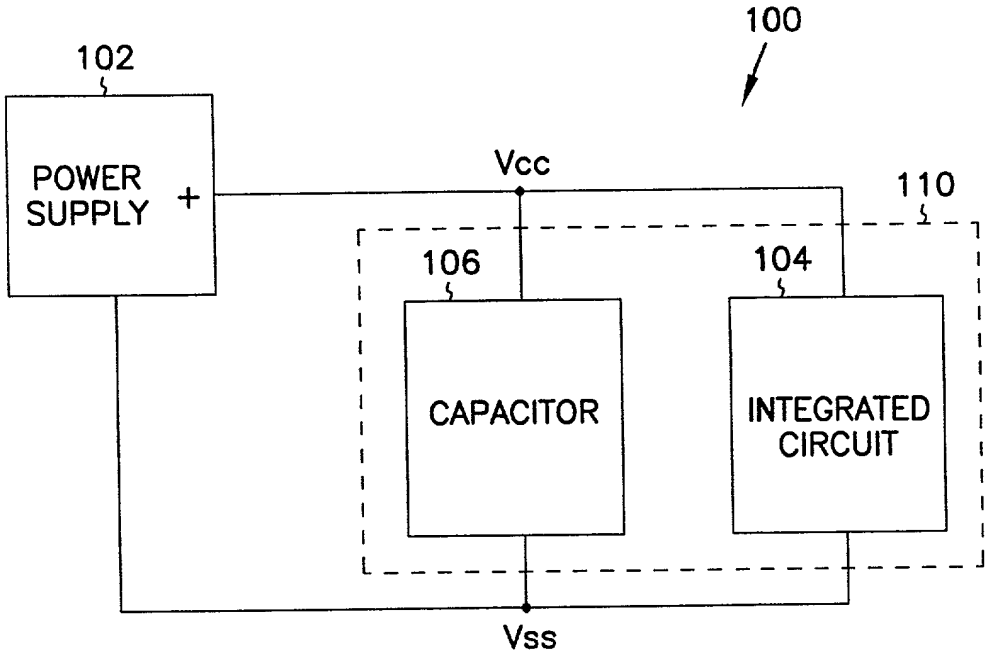
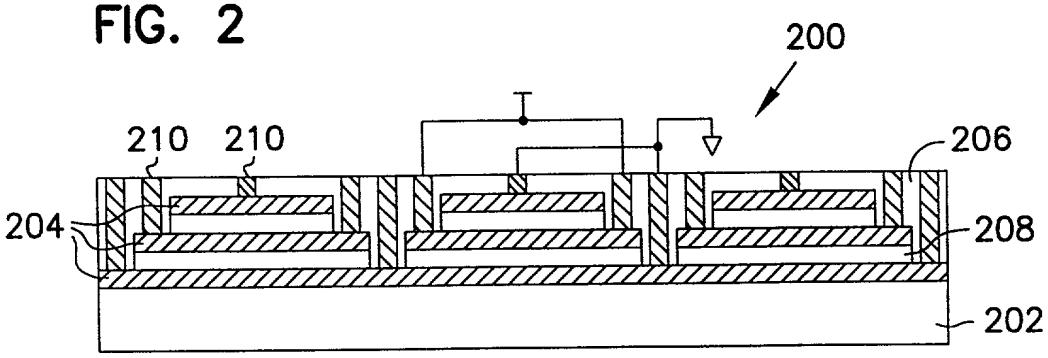

100
102
POWER SUPPLY
+
Vcc
110
106
104
CAPACITOR
INTEGRATED CIRCUIT
Vss

FIG. 1

FIG. 2



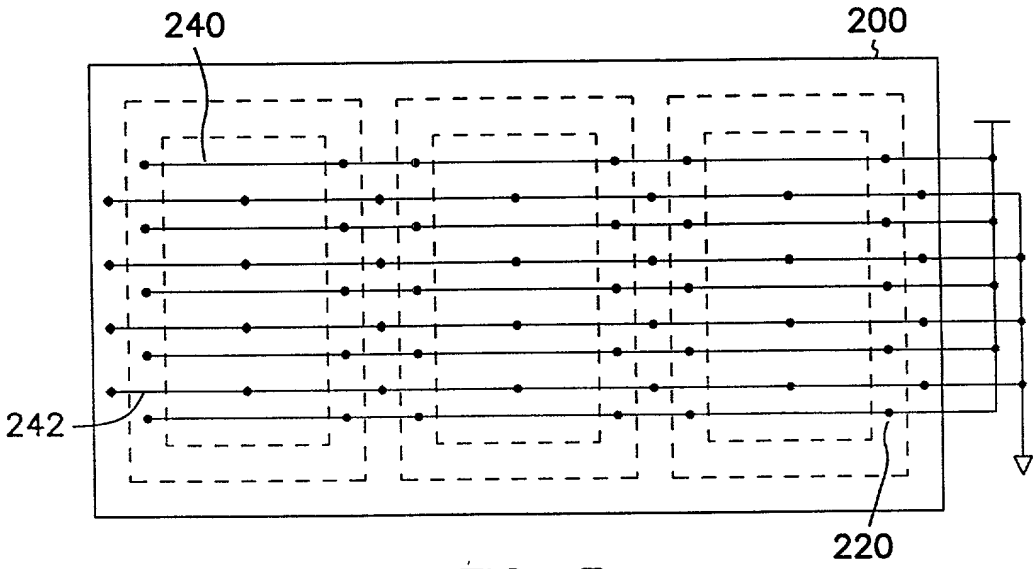


FIG. 3

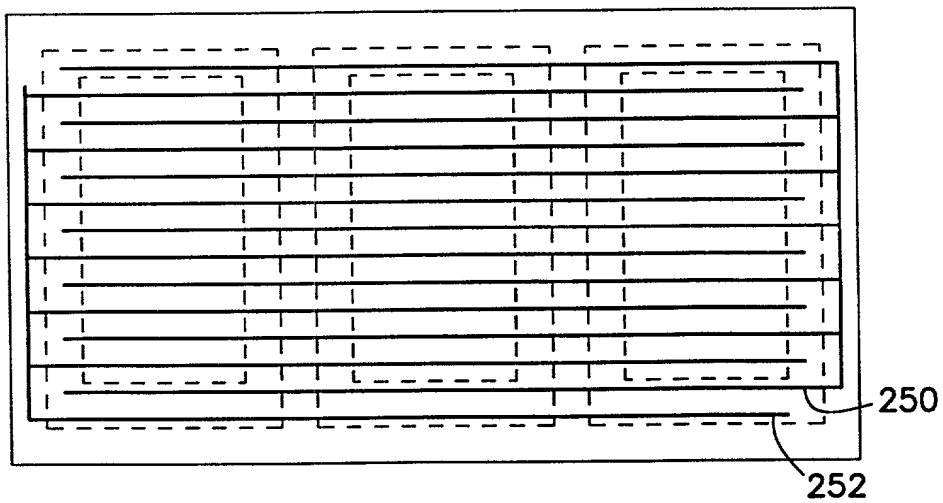


FIG. 4

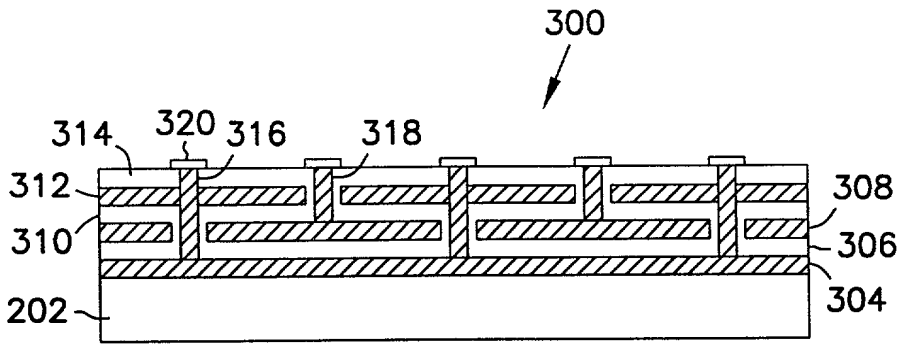


FIG. 5

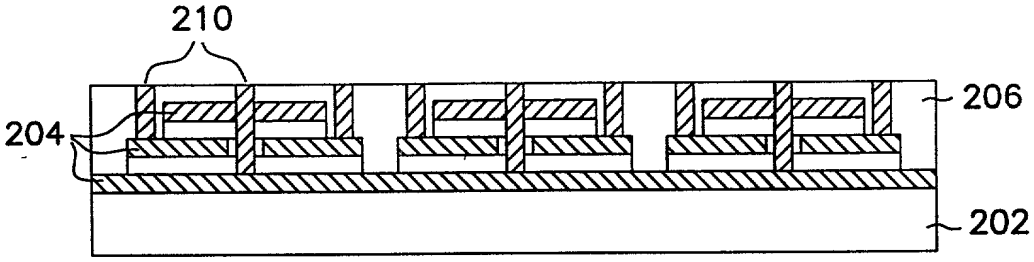


FIG. 6

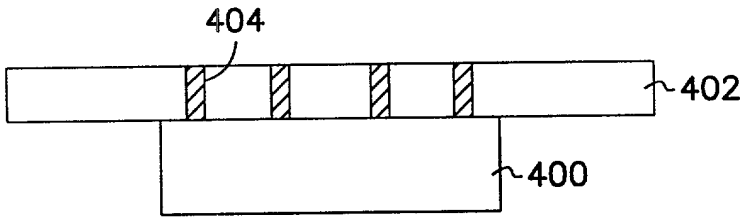


FIG. 7

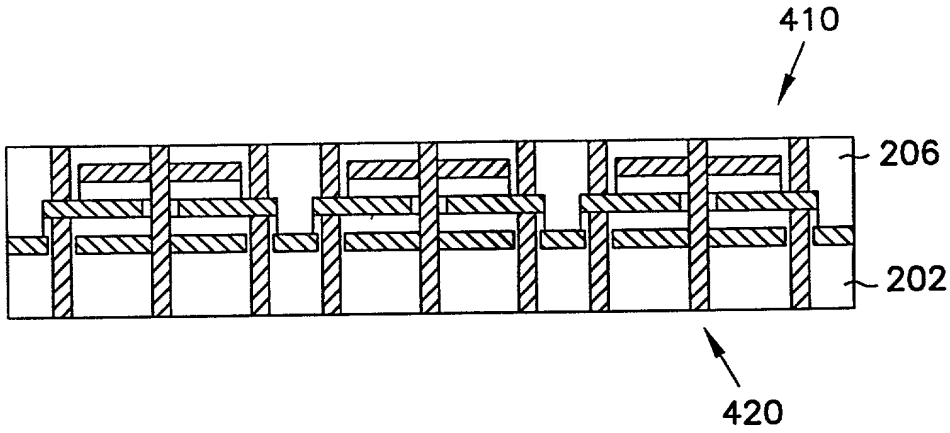


FIG. 8

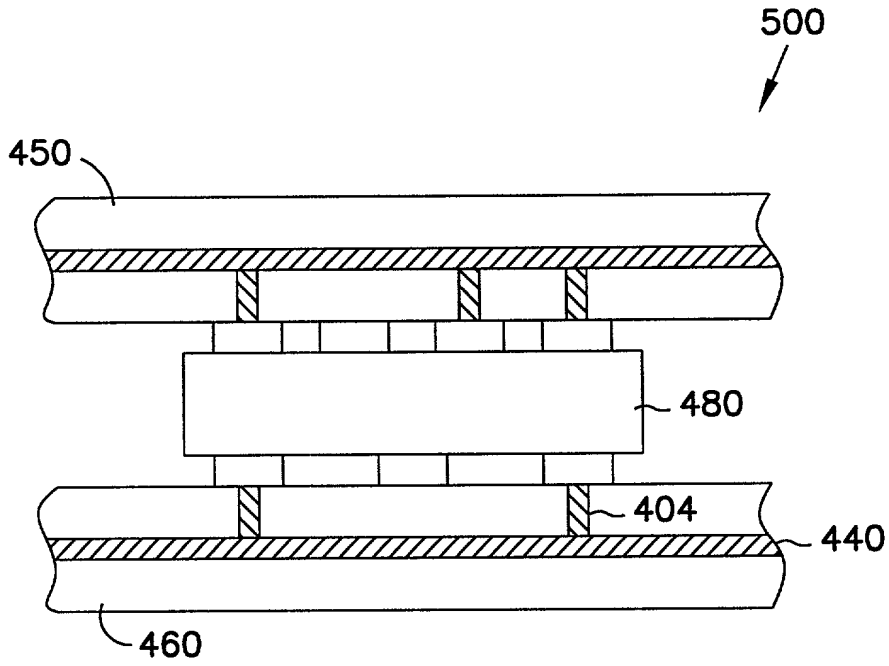


FIG. 9

Attorney Docket No 884.240US1

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **MULTI-LAYER CHIP CAPACITOR**.

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. § 1.56 (attached hereto). I also acknowledge my duty to disclose all information known to be material to patentability which became available between a filing date of a prior application and the national or PCT international filing date in the event this is a Continuation-In-Part application in accordance with 37 C.F.R. §1.63(e).

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 120 or 365(c) of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

No such claim for priority is being made at this time.

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of sole inventor : **Larry Eugene Mosley**
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§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.